What is claimed is:

1. A control unit featuring clocked data transmission between a processor (μC) and at least one further circuit (ASIC 1, 2, n), the processor (μC) outputting a clock pulse (SCKr),
wherein the processor (μC) is configured in such a manner that the processor (μC) monitors the clock pulse (SCKr) based on output signals of at least two clock outputs (10, 11).

2. The control unit as recited in Claim 1,
wherein the at least two clock outputs (10, 11) are connected in such a manner that the control unit generates a monitoring signal as a function of the output signals.

3. The control unit as recited in Claim 2,
wherein an exclusive-OR element (12) is provided to which the output signals are supplied, respectively; the monitoring signal being generated as a function of a signal of the exclusive-OR element (12).

4. The control unit as recited in Claim 1,
wherein the at least two clock outputs (10, 11) are connected in such a manner that the output signals are fed back respectively to a first and a second input (13, 14) of the processor (μC) in order for the processor (μC) to monitor the output signals and to generate the monitoring signal as a function thereof.

5. The control unit as recited in Claim 1,
wherein the at least two clock outputs (10, 11) are connected in such a manner that the clock pulse (SCKr) is generated as a function of the output signals.

6. The control unit as recited in Claim 5,
wherein the at least two clock outputs (10, 11) are ORed together to generate the clock pulse.

7. The control unit as recited in Claim 6,
wherein for ORing the at least two clock outputs (10, 11), a diode (D1, D2) or an OR gate are provided, respectively.

8. The control unit as recited in Claim 6 or 7,
wherein the clock pulse (SCKr) are supplied to an impedance transformer and/or an amplifier (V).

9. The control unit as recited in one of the preceding claims,
wherein the clock outputs (10, 11) are assigned to different port groups.

10. The control unit as recited in one of the Claims 4 through 9,
wherein the first and second inputs (13, 14) are assigned to different port groups.